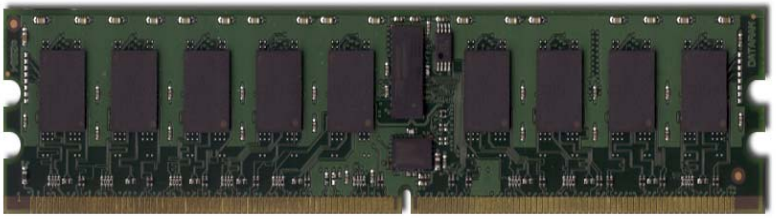
# DTM63310

## 1 GB - 128Mx72, 240-Pin Registered DDR2 DIMM



### Identification

DTM63310 128Mx72

### Performance range

Clock / Module Speed / CL-$t_{RCD}$ -$t_{RP}$

200 MHz / DDR2-400 / 3-3-3

### Features

- 240-pin JEDEC-compliant DIMM
- Operating Voltage: 1.8 V ±0.1
- I/O Type: SSTL_18
- Data Transfer Rate: 400 MHz
- Data Bursts: 4 or 8 bits, Sequential or Interleaved ordering
- Error Checking and Correction (ECC) bits
- Programmable I/O driver strength (OCD)
- Programmable On-Die Termination (ODT)
- Programmable CAS Latency: 3, 4, or 5
- Differential/Single-Ended Data Strobe signals
- SDRAM Addressing (Row/Col/Bank): 14/11/2
- Fully RoHS Compliant

### Description

DTM63310 is a Registered 128Mx72 memory module which conforms to JEDEC's DDR2, PC2-3200 standard. The assembly is comprised of one Rank of eighteen DDR2 DRAMs, two Registers, one Phase-Locked Loop (PLL), and one 2K-bit EEPROM used for Serial Presence Detect.

Both output driver strength and input termination impedance are programmable to maintain signal integrity on the I/O signals. Error Checking and Correction bits are provided to ensure data integrity. The module will support advanced ECC features Chipkill and Intel SDDC.

The eighteen Data Strobe signals may be used either as nine differential pairs, or as eighteen single-ended strobes for use in systems with a mix of x4 and x8 DRAMs.

### Pin Configuration

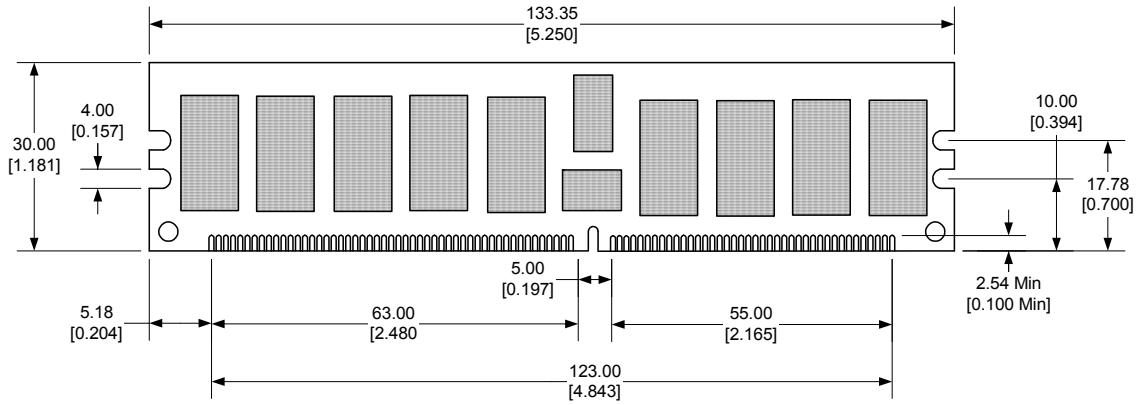
| Front Side | | | | | | | | Back Side | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VREF | 31 | DQ19 | 61 | A4 | 91 | GND | 121 | GND | 151 | GND | 181 | VDD | 211 | DQS14 |
| 2 | GND | 32 | GND | 62 | VDD | 92 | /DQS5 | 122 | DQ4 | 152 | DQ28 | 182 | A3 | 212 | /DQS14 |
| 3 | DQ0 | 33 | DQ24 | 63 | A2 | 93 | DQS5 | 123 | DQ5 | 153 | DQ29 | 183 | A1 | 213 | GND |
| 4 | DQ1 | 34 | DQ25 | 64 | VDD | 94 | GND | 124 | GND | 154 | GND | 184 | VDD | 214 | DQ46 |
| 5 | GND | 35 | GND | 65 | GND | 95 | DQ42 | 125 | DQS9 | 155 | DQS12 | 185 | CK0 | 215 | DQ47 |
| 6 | /DQS0 | 36 | /DQS3 | 66 | GND | 96 | DQ43 | 126 | /DQS9 | 156 | /DQS12 | 186 | /CK0 | 216 | GND |
| 7 | DQS0 | 37 | DQS3 | 67 | VDD | 97 | GND | 127 | GND | 157 | GND | 187 | VDD | 217 | DQ52 |
| 8 | GND | 38 | GND | 68 | Par_In* | 98 | DQ48 | 128 | DQ6 | 158 | DQ30 | 188 | A0 | 218 | DQ53 |
| 9 | DQ2 | 39 | DQ26 | 69 | VDD | 99 | DQ49 | 129 | DQ7 | 159 | DQ31 | 189 | VDD | 219 | GND |
| 10 | DQ3 | 40 | DQ27 | 70 | A10 | 100 | GND | 130 | GND | 160 | GND | 190 | BA1 | 220 | NC |
| 11 | GND | 41 | GND | 71 | BA0 | 101 | SA2 | 131 | DQ12 | 161 | CB4 | 191 | VDD | 221 | NC |
| 12 | DQ8 | 42 | CB0 | 72 | VDD | 102 | NC | 132 | DQ13 | 162 | CB5 | 192 | /RAS | 222 | GND |
| 13 | DQ9 | 43 | CB1 | 73 | /WE | 103 | GND | 133 | GND | 163 | GND | 193 | /S0 | 223 | DQS15 |
| 14 | GND | 44 | GND | 74 | /CAS | 104 | /DQS6 | 134 | DQS10 | 164 | DQS17 | 194 | VDD | 224 | /DQS15 |
| 15 | /DQS1 | 45 | /DQS8 | 75 | VDD | 105 | DQS6 | 135 | /DQS10 | 165 | /DQS17 | 195 | ODT0 | 225 | GND |
| 16 | DQS1 | 46 | DQS8 | 76 | /S1 | 106 | GND | 136 | GND | 166 | GND | 196 | A13 | 226 | DQ54 |
| 17 | GND | 47 | GND | 77 | ODT1 | 107 | DQ50 | 137 | NC | 167 | CB6 | 197 | VDD | 227 | DQ55 |
| 18 | /RESET | 48 | CB2 | 78 | VDD | 108 | DQ51 | 138 | NC | 168 | CB7 | 198 | GND | 228 | GND |
| 19 | NC | 49 | CB3 | 79 | GND | 109 | GND | 139 | GND | 169 | GND | 199 | DQ36 | 229 | DQ60 |
| 20 | GND | 50 | GND | 80 | DQ32 | 110 | DQ56 | 140 | DQ14 | 170 | VDD | 200 | DQ37 | 230 | DQ61 |
| 21 | DQ10 | 51 | VDD | 81 | DQ33 | 111 | DQ57 | 141 | DQ15 | 171 | CKE1 | 201 | GND | 231 | GND |
| 22 | DQ11 | 52 | CKE0 | 82 | GND | 112 | GND | 142 | GND | 172 | VDD | 202 | DQS13 | 232 | DQS16 |
| 23 | GND | 53 | VDD | 83 | /DQS4 | 113 | /DQS7 | 143 | DQ20 | 173 | A15 | 203 | /DQS13 | 233 | /DQS16 |
| 24 | DQ16 | 54 | BA2 | 84 | DQS4 | 114 | DQS7 | 144 | DQ21 | 174 | A14 | 204 | GND | 234 | GND |
| 25 | DQ17 | 55 | /Err_Out* | 85 | GND | 115 | GND | 145 | GND | 175 | VDD | 205 | DQ38 | 235 | DQ62 |
| 26 | GND | 56 | VDD | 86 | DQ34 | 116 | DQ58 | 146 | DQS11 | 176 | A12 | 206 | DQ39 | 236 | DQ63 |
| 27 | /DQS2 | 57 | A11 | 87 | DQ35 | 117 | DQ59 | 147 | /DQS11 | 177 | A9 | 207 | GND | 237 | GND |
| 28 | DQS2 | 58 | A7 | 88 | GND | 118 | GND | 148 | GND | 178 | VDD | 208 | DQ44 | 238 | VDDSPD |
| 29 | GND | 59 | VDD | 89 | DQ40 | 119 | SDA | 149 | DQ22 | 179 | A8 | 209 | DQ45 | 239 | SA0 |
| 30 | DQ18 | 60 | A5 | 90 | DQ41 | 120 | SCL | 150 | DQ23 | 180 | A6 | 210 | GND | 240 | SA1 |

* = Not Used

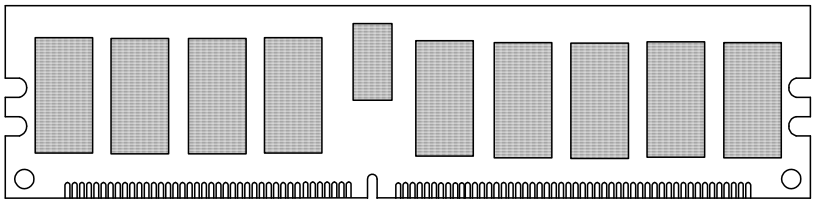
### Pin Description

| Name | Function |
|---|---|
| /CAS | Column Address Strobe |
| /Err_Out* | Parity Error Found |
| /RAS | Row Address Strobe |
| /RESET | Register and PLL Reset |
| /S[1:0] | Chip Selects |
| /WE | Write Enable |
| A[15:0] | Address Inputs |
| BA[2:0] | Bank Addresses |
| CB[7:0] | Data Check Bits |
| CK0, /CK0 | Differential Clock Inputs |
| CKE[1:0] | Clock Enables |
| DQ[63:0] | Data Bits |
| DQS[17:0], /DQS[17:0] | Differential Data Strobes |
| GND | Ground |
| NC | No Connection |
| ODT[1:0] | On Die Termination Inputs |
| Par_In* | Parity Bit, Address & Control |
| SA[2:0] | SPD Address |
| SCL | SPD Clock Input |
| SDA | SPD Data Input/Output |
| VDD | Power |
| VDDSPD | SPD EEPROM Power |
| VREF | Reference Voltage |

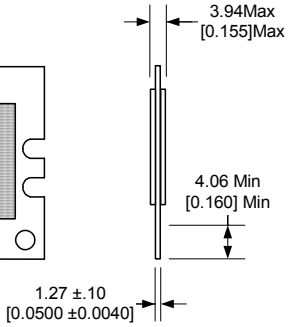
### Front view




### Back view



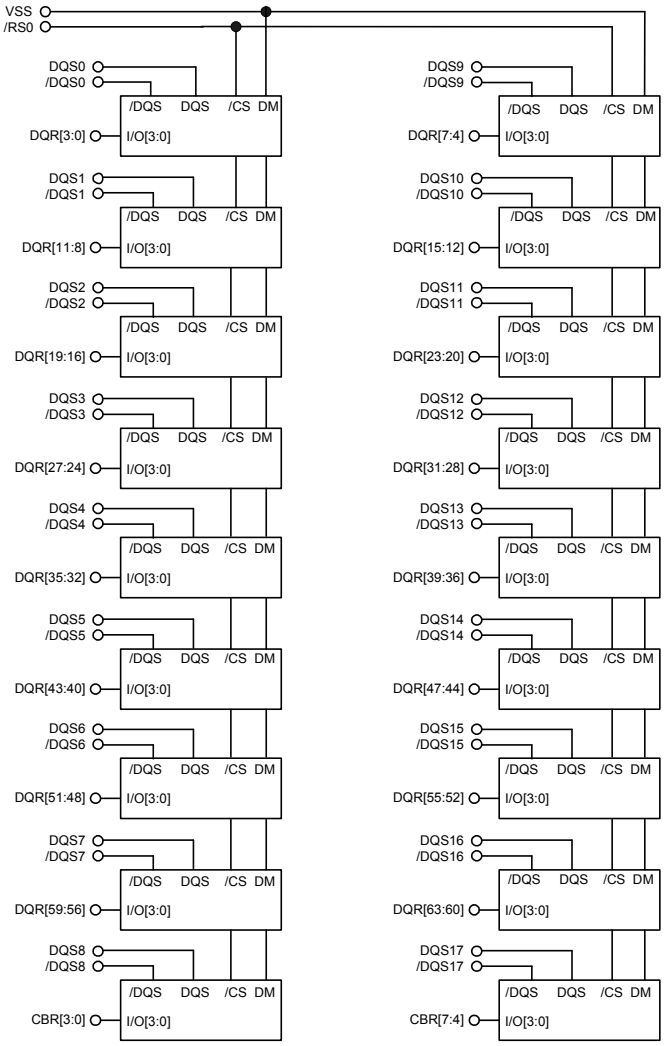
### Side view

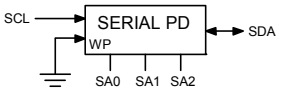



Notes

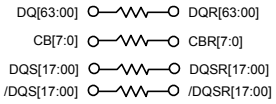
Tolerances on all dimensions except where otherwise indicated are ±.13 (.005).

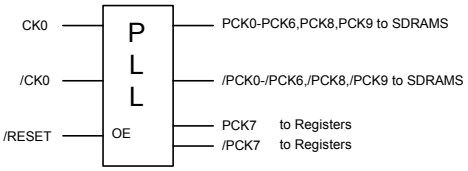
All dimensions are expressed: millimeters [inches]



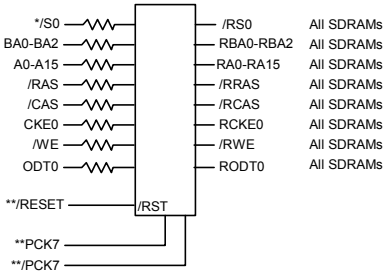




DECOUPLING




REGISTERS




* /S0 connects to /DCS of Register A and /CSR of Register B. /CSR of Register A and /DCS of Register B connect to VDD.

** /RESET, PCK7 and /PCK7 connect to both Registers. Other signals connect to one of two Registers. /S1, CKE1 and ODT1 are NC.

**Notes:**
1. Unless otherwise noted, resistor values are 22 Ohms ±5%

### Absolute Maximum Ratings
(Note: Operation at or above Absolute Maximum Ratings can adversely affect module reliability.)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Temperature, non-Operating** | $T_{STORAGE}$ | -55 | 100 | C |
| **DRAM Case Temperature, Operating** | $T_{CASE}$ | 0 | 85 | C |
| **Voltage on $V_{DD}$ relative to $V_{SS}$** | $V_{DD}$ | -0.5 | 2.3 | V |
| **Voltage on Any Pin relative to $V_{SS}$** | $V_{IN}$,$V_{OUT}$ | -0.5 | 2.3 | V |

### Recommended DC Operating Conditions (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Typical | Maximum | Unit | Note |
|---|---|---|---|---|---|---|
| **Power Supply Voltage** | $V_{DD}$ | 1.7 | 1.8 | 1.9 | V | |
| **I/O Reference Voltage** | $V_{REF}$ | 0.49 $V_{DD}$ | 0.50 $V_{DD}$ | 0.51 $V_{DD}$ | V | 1 |
| **Bus Termination Voltage** | $V_{TT}$ | $V_{REF}$ - 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 | V | |

Notes:
1. The value of $V_{REF}$ is expected to equal one-half $V_{DD}$ and to track variations in the $V_{DD}$ DC level. Peak-to-peak noise on $V_{REF}$ may not exceed ±1% of its DC value.

### DC Input Logic Levels, Single-Ended (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Logical High (Logic 1)** | $V_{IH(DC)}$ | $V_{REF}$ + 0.125 | $V_{DD}$ + 0.300 | V |
| **Logical Low (Logic 0)** | $V_{IL(DC)}$ | -0.300 | $V_{REF}$ - 0.125 | V |

### AC Input Logic Levels, Single-Ended (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| **Logical High (Logic 1)** | $V_{IH(AC)}$ | $V_{REF}$ + 0.250 | - | V |
| **Logical Low (Logic 0)** | $V_{IL(AC)}$ | - | $V_{REF}$ - 0.250 | V |

## Differential Input Logic Levels (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| **DC Input Signal Voltage** | $V_{IN(DC)}$ | -0.300 | $V_{DD}$ + 0.300 | V | 1 |
| **DC Differential Input Voltage** | $V_{ID(DC)}$ | -0.250 | $V_{DD}$ + 0.600 | V | 2 |
| **AC Differential Input Voltage** | $V_{ID(AC)}$ | -0.500 | $V_{DD}$ + 0.600 | V | 3 |
| **AC Differential Cross-Point Voltage** | $V_{IX(AC)}$ | 0.50 VDD - 0.175 | 0.50 VDD + 0.175 | V | 4 |

Notes:
1. $V_{IN(DC)}$ specifies the allowable DC excursion of each input of a differential pair.
2. $V_{ID(DC)}$ specifies the input differential voltage, *i.e.* the absolute value of the difference between the two voltages of a differential pair.
3. $V_{ID(AC)}$ specifies the input differential voltage required for switching.
4. The typical value of $V_{IX(AC)}$ is expected to be 0.5 $V_{DD}$ and is expected to track variations in $V_{DD}$.

## Capacitance (0 C < $T_{CASE}$ < 55 C, f = 100 MHz, $V_{OUT}$(DC) = $V_{DD}$/2, $V_{OUT}$(ac) = 0.1V(p-p))

| PARAMETER | Pin | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| **Input Capacitance, Clock** | CK0, /CK0 | CIN1 | 2 | 3 | pF |
| **Input Capacitance, Address and Control** | BA[1:0], A[12:0], /CS, /RAS, /CAS, /WE, CKE, ODT | CIN2 | 2.5 | 4 | pF |
| **Input/Output Capacitance** | DQ[63:0], CB[7:0], DQS[17:0], /DQS[17:0] | CIO | 3 | 4 | pF |

## DC Characteristics (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Minimum | Maximum | Unit | Note |
|---|---|---|---|---|---|
| **Input Leakage Current** | $I_{LI}$ | -5 | 5 | µA | 1 |
| **Output Leakage Current** | $I_{OZ}$ | -5 | 5 | µA | 2 |
| **Output Minimum Source DC Current** | $I_{OH}$ | -13.4 | - | mA | 3 |
| **Output Minimum Sink DC Current** | $I_{OL}$ | +13.4 | - | mA | 4 |

Notes:
1. These values are guaranteed by design and are tested on a sample basis only
2. DQx and ODT are disabled, and 0 V ≤ $V_{OUT}$ ≤ $V_{DD}$.
3. $V_{DD}$ = 1.7 V, $V_{OUT}$ = 1420 mV. ($V_{OUT}$ - $V_{DD}$)/$I_{OH}$ must be less than 21 Ohms for values of $V_{OUT}$ between $V_{DD}$ and ($V_{DD}$ - 280 mV).
4. $V_{DD}$ = 1.7 V, $V_{OUT}$ = 280 mV. $V_{OUT}$/$I_{OL}$ must be less than 21 Ohms for values of $V_{OUT}$ between 0 V and 280 mV.

## $I_{DD}$ Specifications and Conditions (Voltages referenced to $V_{ss}$ = 0 V)

| PARAMETER | Symbol | Test Condition | Max Value | Unit |
|---|---|---|---|---|
| **Operating One Bank Active-Precharge Current** | $I_{DD}0$ | CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching. | 2520 | mA |
| **Operating One Bank Active-Read-Precharge Current** | $I_{DD}1$ | $I_{OUT}$ = 0 mA; BL = 4, CL = 5 ns, AL = 0; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching. | 2600 | mA |
| **Precharge Power-Down Current** | $I_{DD}2P$ | All banks idle; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. | 530 | mA |
| **Precharge Quiet Standby Current** | $I_{DD}2Q$ | All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating. | 890 | mA |
| **Precharge Standby Current** | $I_{DD}2N$ | All banks idle; CKE is HIGH, /CS is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching. | 1000 | mA |
| **Active Power-Down Current** | $I_{DD}3P$ | All banks open; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. Fast Power-down exit (Mode Register bit 12 = 0) | 980 | mA |
| **Active Power-Down Current** | $I_{DD}3P$ | All banks open; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating. Slow Power-down exit (Mode Register bit 12 = 1) | 710 | mA |
| **Active Standby Current** | $I_{DD}3N$ | All banks open; $t_{RAS}$ = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching. | 1630 | mA |
| **Operating Burst Write Current** | $I_{DD}4W$ | All banks open, Continuous burst writes; BL = 4, CL = 3 $t_{CK}$, AL = 0; $t_{RAS}$ = 70 ms, CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching. | 2800 | mA |
| **Operating Burst Read Current** | $I_{DD}4R$ | All banks open, Continuous burst reads, $I_{OUT}$ = 0 mA; BL = 4, CL = 3 $t_{CK}$, AL = 0; xx, $t_{RAS}$ = 70 ms; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching. | 2980 | mA |
| **Burst Refresh Current** | $I_{DD}5$ | Refresh command at every 75 ns; CKE is HIGH, /CS is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching. | 3790 | mA |
| **Self Refresh Current** | $I_{DD}6$ | CK and /CK at 0 V; CKE ≤ 0.2 V; Other control and address bus inputs are floating; Data bus inputs are floating. | 290 | mA |
| **Operating Bank Interleave Read Current** | $I_{DD}7$ | All bank interleaving reads, $I_{OUT}$= 0 mA; BL = 4, CL = 3 $t_{CK}$; AL = 70 ns; $t_{RRD}$ = 7.5 ns; CKE is HIGH, /CS is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching. | 5230 | mA |

Notes: 1. For all $I_{DD}X$ measurements, $t_{CK}$ = 5 ns, $t_{RC}$ = 60 ns, $t_{RCD}$ = 15 ns, $t_{RAS}$ = 45 ns, and $t_{RP}$ = 15 ns unless otherwise specified.
2. All $I_{DD}X$ values shown are worst-case maximums, considering all DRAMs, Registers, and the PLL.

## AC Operating Conditions

| PARAMETER | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| DQ Output Access Time from Clock | $t_{AC}$ | 0.60 | - | ns |
| CAS-to-CAS Command Delay | $t_{CCD}$ | 2 | - | $t_{CK}$ |
| Clock High Level Width | $t_{CH}$ | 0.45 | 0.55 | $t_{CK}$ |
| Clock Cycle Time | $t_{CK}$ | 5000 | 8000 | ps |
| Clock Low Level Width | $t_{CL}$ | 0.45 | 0.55 | $t_{CK}$ |
| Data Input Hold Time after DQS Strobe | $t_{DH}$ | 0.28 | - | ns |
| DQ Input Pulse Width | $t_{DIPW}$ | 0.35 | - | $t_{CK}$ |
| DQS Output Access Time from Clock | $t_{DQSCK}$ | -500 | +500 | ps |
| Write DQS High Level Width | $t_{DQSH}$ | 0.35 | - | $t_{CK}$ |
| Write DQS Low Level Width | $t_{DQSL}$ | 0.35 | - | $t_{CK}$ |
| DQS-Out Edge to Data-Out Edge Skew | $t_{DQSQ}$ | 350 | - | ps |
| Data Input Setup Time Before DQS Strobe | $t_{DS}$ | 0.15 | - | ns |
| DQS Falling Edge from Clock, Hold Time | $t_{DSH}$ | 0.2 | - | $t_{CK}$ |
| DQS Falling Edge to Clock, Setup Time | $t_{DSS}$ | 0.2 | - | $t_{CK}$ |
| Clock Half Period | $t_{HP}$ | minimum of $t_{CH}$ or $t_{CL}$ | - | ns |
| Address and Command Hold Time after Clock | $t_{IH}$ | 0.5 | - | ns |
| Address and Command Setup Time before Clock | $t_{IS}$ | 0.5 | - | ns |
| Load Mode Command Cycle Time | $t_{MRD}$ | 2 | - | $t_{CK}$ |
| DQ-to-DQS Hold | $t_{QH}$ | $t_{HP}$ - $t_{QHS}$ | - | - |
| Data Hold Skew Factor | $t_{QHS}$ | 450 | - | ps |
| Active-to-Precharge Time | $t_{RAS}$ | 45 | 120K | ns |
| Active-to-Active / Auto Refresh Time | $t_{RC}$ | 60 | - | ns |
| RAS-to-CAS Delay | $t_{RCD}$ | 15 | - | ns |
| Average Periodic Refresh Interval | $t_{REFI}$ | - | 7.8 | µs |
| Auto Refresh Row Cycle Time | $t_{RFC}$ | 75 | - | ns |
| Row Precharge Time | $t_{RP}$ | 15 | - | ns |
| Read DQS Preamble Time | $t_{RPRE}$ | 0.9 | 1.1 | $t_{CK}$ |
| Read DQS Postamble Time | $t_{RPST}$ | 0.4 | 0.6 | $t_{CK}$ |
| Row Active to Row Active Delay | $t_{RRD}$ | 7.5 | - | ns |
| Internal Read to Precharge Command Delay | $t_{RTP}$ | 7.5 | - | ns |
| Write DQS Preamble Setup Time | $t_{WPRES}$ | 0 | - | ps |
| Write DQS Postamble Time | $t_{WPST}$ | 0.4 | 0.6 | $t_{CK}$ |
| Write Recovery Time | $t_{WR}$ | 15 | - | ns |
| Internal Write to Read Command Delay | $t_{WTR}$ | 10 | - | ns |
| Exit Self Refresh to Non-Read Command | $t_{XSNR}$ | $t_{RFC}$(min) + 10 | - | ns |
| Exit Self Refresh to Read Command | $t_{XSRD}$ | 200 | - | $t_{CK}$ |

## Serial Presence Detect Contents

| Byte# | Function | Value | Hex |
|---|---|---|---|
| 0 | Number of Serial PD Bytes written during module production | 128 bytes | 80 |
| 1 | Total number of Bytes in Serial Presence Detect device | 256 bytes | 08 |
| 2 | Fundamental Memory Type | DDR2 | 08 |
| 3 | Number of Row Addresses | 14 | 0E |
| 4 | Number of Column Addresses | 11 | 0B |
| 5 | Module Attributes - Number of Ranks, Package and Height | | 60 |
| | bits 0 through 2 - number of Ranks | 1 | |
| | bit 3 - Card on Card | No | |
| | bit 4 - DRAM Package | Planar | |
| | bits 5 through 7 - Module Height | 30mm | |
| 6 | Module Data Width | 72 | 48 |
| 7 | Reserved | UNUSED | 00 |
| 8 | Voltage Interface Level of this assembly | SSTL/1.8V | 05 |
| 9 | SDRAM Cycle time at highest CAS Latency | 5 ns | 50 |
| 10 | SDRAM Access from Clock time at highest CAS Latency ($t_{AC}$) | 0.6 ns | 60 |
| 11 | DIMM configuration type | ECC | 02 |
| 12 | Refresh Rate/Type | 7.8 µs<br>Self Refresh | 82 |
| 13 | Primary SDRAM Width | 4 | 04 |
| 14 | Error Checking SDRAM Width | 4 | 04 |
| 15 | Reserved | UNUSED | 00 |
| 16 | SDRAM Device Attributes - Burst Lengths Supported | | 0C |
| | bits 0 and 1 - [undefined] | | |
| | bit 2 - Burst Length = 4 | yes | |
| | bit 3 - Burst Length = 8 | yes | |
| | bits 4 through 7 - [undefined] | | |
| 17 | SDRAM Device Attributes - Number of Banks on SDRAM Device | 4 | 04 |
| 18 | SDRAM Device Attributes - CAS Latency | | 38 |
| | bits 0 and 1 - [undefined] | | |
| | bit 2 - Latency = 2 | | |
| | bit 3 - Latency = 3 | yes | |
| | bit 4 - Latency = 4 | yes | |
| | bit 5 - Latency = 5 | yes | |
| | bits 6 and 7 - [undefined] | | |
| 19 | Reserved | UNUSED | 00 |
| 20 | DIMM type information | | 01 |
| | bit 0 - Regular RDIMM (133.35mm) | yes | |
| | bit 1 - Regular UDIMM (133.35mm) | no | |
| | bit 2 - SODIMM (67.6mm) | no | |
| | bit 3 - Micro-DIMM (45.5mm) | no | |
| | bit 4 - Mini RDIMM (82.0mm) | no | |
| | bit 5 - Mini UDIMM (82.0mm) | no | |
| | bits 6 and 7 - [undefined] | no | |
| 21 | Module Attributes | | 00 |
| | bits 0 through 3 - [undefined] | | |
| | bit 4 - FET Switch External Enable | no | |
| | bit 5 - [undefined] | | |
| | bit 6 - Analysis probe installed | no | |
| | bit 7 - [undefined] | | |
| 22 | SDRAM Device Attributes - General | | 00 |
| | bit 0 - Supports Weak Driver | no | |
| | bits 1 through 7 - [undefined] | | |
| 23 | Minimum Clock Cycle Time at Reduced CAS Latency, CL = X-1 | 5 ns | 50 |
| 24 | Maximum Data Access Time ($t_{AC}$) from Clock at CL = X-1 | 0.6 ns | 60 |

| | | | |
|---|---|---|---|
| 25 | Minimum Clock Cycle Time at Reduced CAS Latency CL = X-2 | 5 | 50 |
| 26 | Maximum Data Access Time ($t_{AC}$) from Clock at CL = X-2 | 0.6 | 60 |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 15 ns | 3C |
| 28 | Minimum Row Active to Row Active Delay ($t_{RRD}$) | 7.5 ns | 1E |
| 29 | Minimum RAS to CAS Delay ($t_{RCD}$) | 15 ns | 3C |
| 30 | Minimum Active to Precharge Time ($t_{RAS}$) | 45 ns | 2D |
| 31 | Module Rank Density | 1 GB | 01 |
| 32 | Address and Command Setup Time before Clock ($t_{IS}$) | 0.50 ns | 50 |
| 33 | Address and Command Hold Time after Clock ($t_{IH}$) | 0.50 ns | 50 |
| 34 | Data Input Setup Time before Strobe ($t_{DS}$) | 0.15 ns | 15 |
| 35 | Data Input Hold Time after Strobe ($t_{DH}$) | 0.28 ns | 28 |
| 36 | Write Recovery Time ($t_{WR}$) | 15 ns | 3C |
| 37 | Internal Write-to-Read Command Delay ($t_{WTR}$) | 10 ns | 28 |
| 38 | Internal Read-to-Precharge Command Delay ($t_{RTP}$) | 7.5 ns | 1E |
| 39 | Memory Analysis Probe Characteristics. | UNUSED | 00 |
| 40 | Extension of Byte 41($t_{RC}$) and Byte 42 ($t_{RFC}$) | | 00 |
| | Add this value to byte 41 | 0 ns | |
| | Add this value to byte 42 | 0 ns | |
| 41 | Minimum Active-to-Active / Auto Refresh Time ($t_{RC}$) | 60 ns | 3C |
| 42 | Minimum Auto-Refresh to Active/Auto-Refresh Command Period ($t_{RFC}$) | 105 ns | 69 |
| 43 | Maximum Cycle Time ($t_{CK}$ max) | 8 ns | 80 |
| 44 | DQS-DQ Skew for DQS & associated DQ Signals ($t_{DQSQ}$) | 0.35 ns | 23 |
| 45 | Read Data Hold Skew Factor ($t_{QHS}$) | 0.45 ns | 2D |
| 46 | PLL Relock Time | 15 µs | 0F |
| 47-61 | Reserved | UNUSED | 00 |
| 62 | SPD Revision | Revision 1.0 | 10 |
| 63 | Checksum for Bytes 0-62 | checksum | F2 |
| 64 | Module Manufacturer's JEDEC ID Code | Dataram ID | 7F |
| 65 | Module Manufacturer's JEDEC ID Code | Dataram ID | 91 |
| 66-71 | Module Manufacturer's JEDEC ID Code | UNUSED | 00 |
| 72 | Module Manufacturing Location | UNUSED | 00 |
| 73-90 | Module Part Number | UNUSED | 00 |
| 91-92 | Module Revision Code | UNUSED | 00 |
| 93-94 | Module Manufacturing Date | UNUSED | 00 |
| 95-98 | Module Serial Number | [serial number] | |
| 99-127 | Manufacturer's Specific Data | UNUSED | 00 |

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